WHAT IS CLAIMED IS:

1. A method for analyzing circuit designs, comprising the steps of:

discretizing a design representation into pixel elements representative of a structure in the design;

determining at least one property for each pixel element representing a portion of the design; and

determining a response of the design due to local properties across the design.

2. The method as recited in claim 1, further comprising the step of exporting pixel properties to an application.

3. The method as recited in claim 1, further comprising the step of assembling pixel properties to determine local three-dimensional properties.

4. The method as recited in claim 3, wherein the step of determining a response of the design due to local

properties across the design includes the step of determining a global response for an architecture due to the local three-dimensional properties.

5. The method as recited in claim 1, further comprising the step of importing a design to be analyzed.

6. The method as recited in claim 5, wherein the design includes a computer generated design of one of a circuit and a chip.

7. The method as recited in claim 1, wherein the at least one property includes metal fraction and the global response includes thermal strain.

8. The method as recited in claim 1, wherein the step of determining a response of the design includes accepting or rejecting a design based on the response.

9. The method as recited in claim 8, further

comprising the step of altering a design based on the response.

10. The method as recited in claim 1, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

11. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs, as recited in claim 1.

12. The method as recited in claim 1, wherein the at least one property includes metal fraction information relating to the metal fraction is generated for the location and number of stacked via structures.

13. A method for analyzing circuit designs,

comprising the steps of:

discretizing a design representation into pixel elements representative of a structure in the design;

analyzing properties in each pixel element;

assembling pixel properties to determine properties of a local three-dimensional circuit architecture; and

determining a global response of the circuit architecture due to local properties across the design.

14. The method as recited in claim 13, further comprising the step of exporting pixel properties to an application.

15. The method as recited in claim 13, further comprising the step of importing a design to be analyzed.

16. The method as recited in claim 15, wherein the design includes a computer generated design of one of a circuit and a chip.

17. The method as recited in claim 13, wherein at least one property includes metal fraction and the global response includes thermal strain.

18. The method as recited in claim 13, wherein the step of determining a global response of the design includes accepting or rejecting a design based on the global response.

19. The method as recited in claim 18, further comprising the step of altering a design based on the global response.

20. The method as recited in claim 13, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

21. A program storage device readable by machine,

tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs, as recited in claim 13.

22. The method as recited in claim 13, wherein the at least one property includes metal fraction information relating to the metal fraction is generated for the location and number of stacked via structures.

23. A method for analyzing circuit designs, comprising the steps of:

importing a digitally rendered representation of a design;

discretizing the design representation into pixel elements representative of a structure in the design;

analyzing properties in each pixel element by calculating the properties based on geometrical features in the design;

assembling pixel properties in geometrical regions to determine properties of a local three-dimensional circuit

architecture; and

determining a global response of the circuit architecture due to the local properties across the design.

24. The method as recited in claim 23, further comprising the step of exporting pixel properties to an application.

25. The method as recited in claim 23, wherein the design includes the design of a circuit or a chip.

26. The method as recited in claim 23, wherein at least one property includes metal fraction and the global response includes thermal strain.

27. The method as recited in claim 23, wherein the step of determining a global response of the design includes accepting or rejecting a design based on the global response.

28. The method as recited in claim 23, further comprising the step of altering a design based on the global response.

29. The method as recited in claim 23, wherein the step of determining a response further includes representing a three-dimensional multi-layered design in two dimensions such that properties within all layers are accumulated and represented in the two-dimensional image.

30. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for analyzing circuit designs, as recited in claim 23.

31. The method as recited in claim 23, wherein the at least one property includes metal fraction information relating to the metal fraction is generated for the location and number of stacked via structures.